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# Fully Depleted and Backside Biased Monolithic CMOS Image Sensor

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## ABSTRACT

We are presenting a novel concept for a fully depleted, monolithic, pinned photodiode CMOS image sensor using reverse substrate bias. The principle of operation allows the manufacture of backside illuminated CMOS sensors with active thickness in excess of 100  $\mu\text{m}$ . This helps increase the QE at near-IR and soft X-ray wavelengths, while preserving the excellent characteristics associated with the pinned photodiode sensitive elements. Such sensors are relevant to a wide range of applications, including scientific imaging, astronomy, Earth observation and surveillance.

A prototype device with 10  $\mu\text{m}$  and 5.4  $\mu\text{m}$  pixels using this concept has been designed and is being manufactured on a 0.18  $\mu\text{m}$  CMOS image sensor process. Only one additional implantation step has been introduced to the normal manufacturing flow to make this device. The paper discusses the design of the sensor and the challenges that had to be overcome to realise it in practice, and in particular the method of achieving full depletion without parasitic substrate currents. It is expected that this new technology can be competitive with modern backside illuminated thick CCDs for use at visible to near-IR telescopes and synchrotron light sources.

**Keywords:** CMOS image sensor (CIS), full depletion, pinned photodiode (PPD), high quantum efficiency.

## 1. INTRODUCTION

The commercial and scientific applications of CMOS active pixel image sensors (CIS) are increasing constantly, benefiting from the great improvements in performance that have occurred over the last 10-15 years. Despite the advances in CMOS technology, many areas are not yet served by CIS, and CCDs still dominate where the highest performance is required. In contrast, consumer imaging is now almost entirely the domain of CIS.

The pinned photodiode (PPD)<sup>1</sup> was the single most important development over the last decade to enable CIS to reach the performance levels of the CCDs. Originally invented<sup>2</sup> for CCDs in the 1980s, PPD technology was applied to CIS by a number of companies and it is mass produced today. This allowed the implementation of efficient correlated double sampling (CDS), a key ingredient for reducing the readout noise. Furthermore, backside illumination (BSI) was added to CIS in order to boost the QE, remove the reflections from front side metal layers, and increase the fill factor. The integration of analogue and digital blocks in CIS allows high frame rate readout with low noise due to the parallelism of the readout chain, something that is not possible in a monolithic CCD process.

Devices with high QE, large sensitive area and low readout noise are required for space and science applications. CIS already demonstrate excellent readout noise levels reaching single electrons RMS, and large devices can be made. However, their QE is not yet competitive due to the relatively thin sensitive layer, usually below 10  $\mu\text{m}$ . Figure 1 shows the QE of a modern BSI CIS (e.g. e2v Technologies CIS115)<sup>3</sup> and the expected improvements resulting from using thick, fully depleted substrate. For good sensitivity in the red and near-IR, sensors with thicknesses of at least 50  $\mu\text{m}$  are required (e.g. Gaia red, and Euclid VIS CCDs), and typical thicknesses are in the 100-200  $\mu\text{m}$  range (e.g. the CCD sensors for LSST). High QE is particularly important for high speed imaging, for example in adaptive optics systems, where the signal levels are naturally low due to the short integration times. High speed imaging is an area where CMOS image sensors excel over CCDs, and QE improvements are very desirable. CIS are already under consideration for high speed adaptive optics at future telescopes, with ESO conducting a development programme for E-ELT using traditional CIS<sup>4</sup>. In addition, high red sensitivity is required for hyperspectral and other Earth observation imagers, as well as for surveillance.

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Much thicker sensitive volume needs to be depleted to increase the QE of CIS, and that requires bias voltages far higher than the typically used in CMOS devices. Backside biasing is a good way to achieve that without affecting the pixel circuitry, and allows sensors with thicknesses of several hundred micrometres to be realised. Unlike CCDs, where backside biasing is well established, the presence of active transistors in the CMOS pixel makes backside biasing far more complex and significant development is required to achieve it.

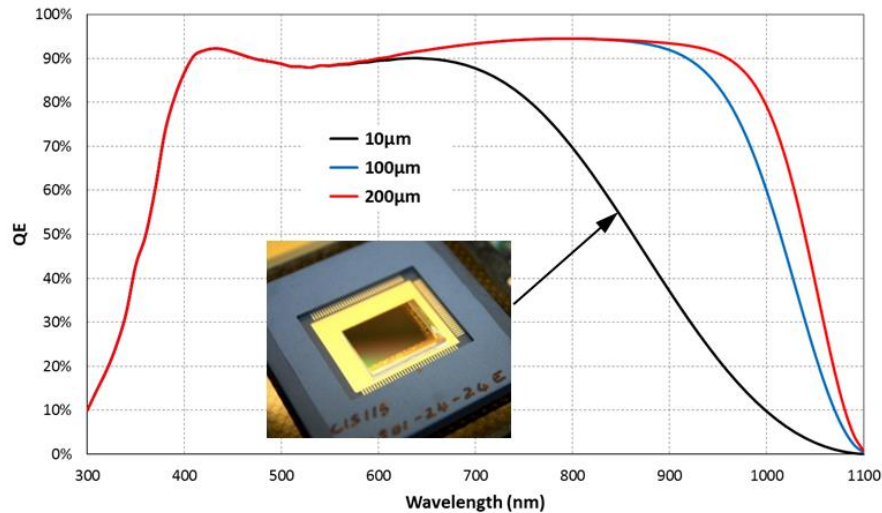


Figure 1 – Calculated QE of silicon image sensors with thickness of 100µm and 200 µm, compared to the state of the art 10 µm thick CIS115 (inset).

The main challenge in designing a backside biased PPD CIS, as will be described later on, is the prevention of leakage current between the front side p-wells, containing the pixel transistors, and the substrate. This paper details the approach we have taken in solving this problem and the solution implemented in a prototype CIS.

## 2. PIXEL STRUCTURE

### 2.1 The Pinned Photodiode (PPD) pixel

The PPD pixel (also known as 4T) consists of four n-channel MOS transistors, as shown in Figure 2. Transistor T1 is used to reset the sense node to the reference voltage applied at the RD terminal, the source follower T2 buffers the sense node voltage, and T3 acts as a switch to connect the source of T2 to the column readout line. Applying a voltage pulse to the gate of T4 transfers the charge collected in the photodiode to the sense node.

With PPD pixels it is possible to remove the reset noise due to the separation of the charge collection element, the photodiode, from the charge sensing element, the sense node. The sense node is reset shortly before the charge is transferred to it, and its voltage is sampled. After the charge transfer the sense node is sampled again, and the difference between the two voltage samples contains the signal without the reset noise.

All transistors are placed in a p-well within the pixel boundaries. Normally, the in-pixel p-well is at the same potential as the substrate. Attempting to alter the bias of the p-well is potentially problematic due to the finely tuned charge transfer from the photodiode to the sense node and its sensitivity to the bias and clock levels. Transferring the collected charge from the photodiode to the sense node FD quickly and without significant lag is one of the most critical aspects of any PPD pixel design.

The potential at the surface of the PPD is fixed (pinned) to substrate potential due to the heavily doped p+ implant. The peak potential under the photodiode, referred to as the pinning potential  $V_{pin}$ , is typically in the range 1.0-2.0V, and is controlled by the doping profile of the diode. To first order, the structure of the PPD could be approximated with a pn junction with a cathode biased at  $V_{pin}$ .

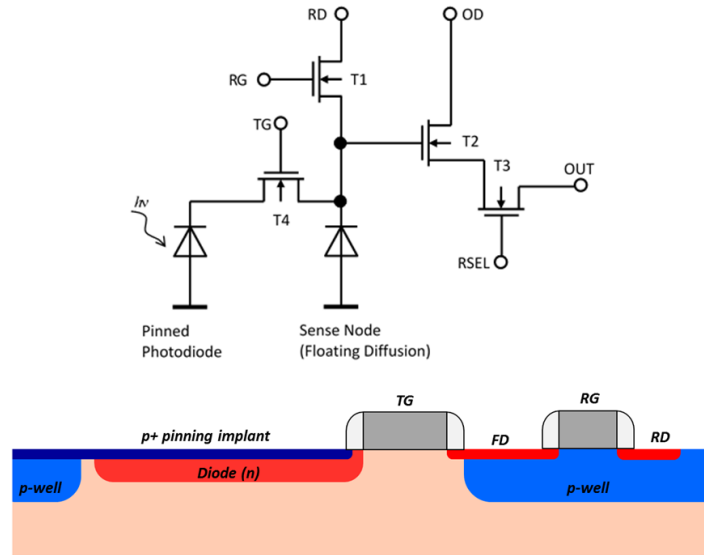


Figure 2 – Schematic of a PPD pixel and a cross sectional diagram along the direction of charge transfer. Only T1 and T4 are shown in the physical diagram.

## 2.2 Reverse bias to a PPD pixel

When implementing fully depleted structure it is desirable to keep the operating conditions of the PPD unaltered, and change the substrate bias instead. If the substrate of a normal PPD pixel is reverse biased relative to the in-pixel p-well, reverse current starts to flow due to the resistive path p+-p-p+ connecting the front and the back of the structure, as shown in Figure 3. This current can be very large and should be completely eliminated in a practical device.

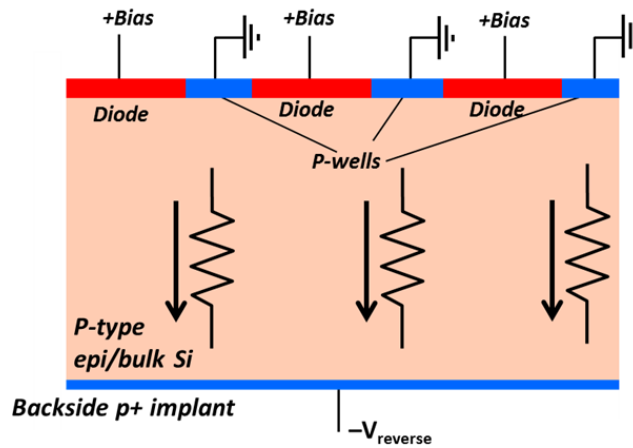


Figure 3 – Leakage current between the front side p-wells and the backside of a reverse biased PPD pixel structure.

The reason for the leakage current is that the depletion regions created under the PPDs usually do not merge, as shown in Figure 4. This can be explained by the low  $V_{pin}$ , and that the typical p-wells lie much deeper than the PPDs and are

heavily doped. If a pinch-off can be achieved, the conductive path from the p-wells to the backside p+ contact can be cut off and the leakage current eliminated.

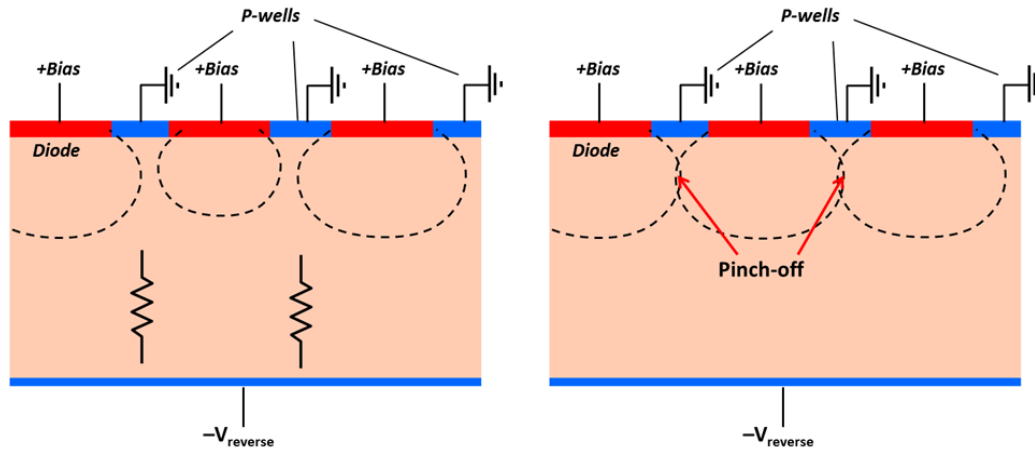


Figure 4 – Leakage current and its elimination by pinch-off.

Achieving pinch-off depends on many factors, such as the size, depth and doping profiles of the PPD and the p-wells, the pinning voltage and the amount of charge collected under PPD. As more charge is collected, the peak potential under the PPD is reduced, which could break the pinch-off and allow leakage currents to flow.

As a first measure to ensure pinch-off under all conditions, the p-wells should be made as narrow and shallow as possible. However, there are limitations in doing this due to the need to place 4 transistors in them, and ultimately it may not be sufficient to prevent the leakage current.

### 2.3 Deep depletion extension

After a detailed study of the PPD structure using semiconductor device simulations, we have arrived at the design shown in Figure 5. Additional n-type implants, called Deep Depletion Extension (DDE), are placed under the p-wells with the purpose to help extend the depletion regions formed under the PPDs sideways towards and underneath the p-wells, and thus to facilitate pinch-off. The DDE implant is not in contact with the PPDs, and is relatively lightly doped.

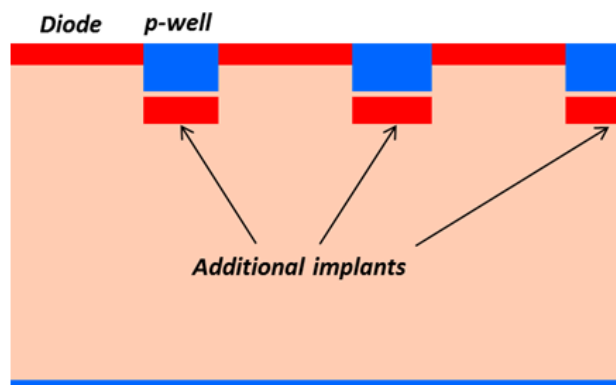


Figure 5 – Proposed implant structure for ensuring pinch-off.

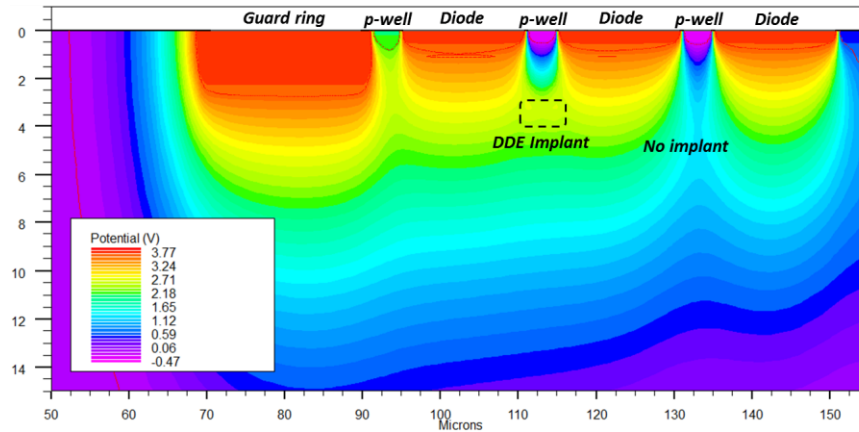


Figure 6 – Potential profile in a 2D, 3-pixel PPD model showing the effect of the DDE implant under the second p-well.

The equipotential lines in the simulation model in Figure 6 show how the depletion regions under the first and the second diodes have merged in the area where the DDE is implanted, and how this does not happen where the DDE is absent. The p-wells above the pinched-off areas do not have a conductive path via the substrate and this prevents leakage currents when the substrate is reverse biased.

Applying reverse bias to this structure is usually accomplished via a front face contact as it is much more convenient than a dedicated contact to the back side. Figure 7 shows the typical arrangement, applicable to a number of CMOS and CCD image sensors. The silicon under the substrate ring is kept undepleted by making the distance  $A$  to the guard ring sufficiently large to ensure that the depleted region does not extend under the substrate ring. In addition, the distance  $A$  should be chosen so as to prevent avalanche breakdown between the substrate and the guard rings. As a rule of thumb, the distance  $A$  should be approximately equal to the substrate thickness  $D$ .

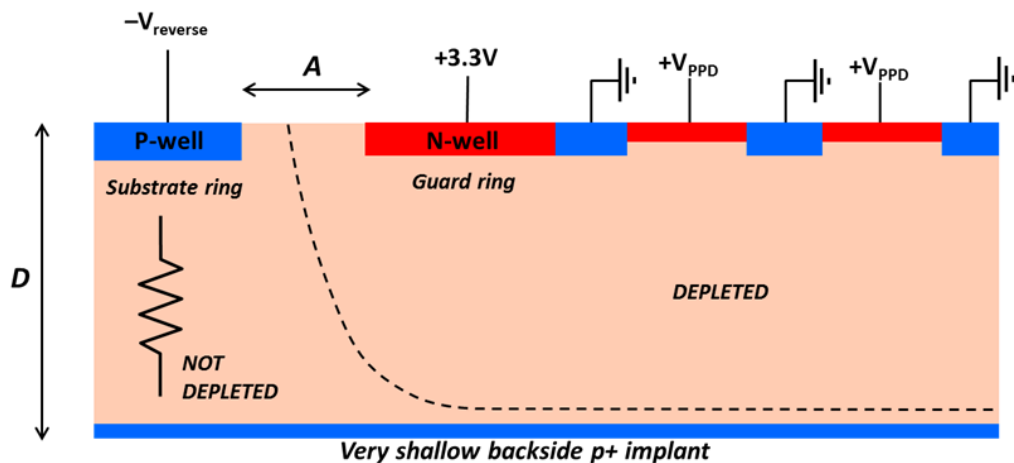


Figure 7 – Reverse biasing of an image sensor using a front side contact.

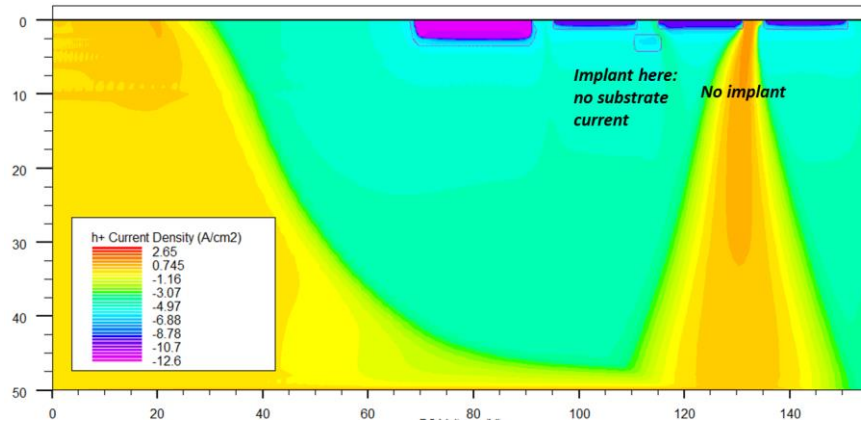


Figure 8 – Hole current density in a 3-pixel simplified PPD model. The dimensions are in micrometers.

Figure 8 shows the simulated hole current for the 3-pixel model in Figure 6, reverse biased at -20V. The negative substrate potential is applied from the front through an undepleted part of the substrate as shown in Figure 7, and the front side p-wells are biased at 0V. The presence of the DDE implant completely stops the front-to-back leakage current. In contrast, the simulation shows the substantial hole current resulting from a pixel where the DDE is omitted.

### 3. PROTOTYPE DEVICE

#### 3.1 Design

Based on the proof of principle simulations outlined above, we designed a prototype device based on the single poly, 4 level metal PPD (4T) 0.18  $\mu\text{m}$  CIS process from TowerJazz Semiconductor. This process is well established and produces CIS with excellent electro-optical characteristics for scientific and space applications.

Two pixels were designed, using existing 10  $\mu\text{m}$  and 5.4  $\mu\text{m}$  4T layouts, and the DDE implant was simulated in TCAD software in 2D and 3D using simplified GDSII geometry. Simulations were carried out to determine the optimum size, depth and the doping concentration of the new implant.

Efforts were concentrated on the refinement of the initial simulations shown above and on exploring the effects on  $V_{\text{pin}}$ , depletion depth and leakage currents. Unlike the simplified 2D models where the PPD is represented by a pn junction, real PPDs are non-equilibrium devices similar to a CCD pixel and require more complex, non-stationary simulation.

In a PPD the pinning voltage is not fixed by the bias at the cathode of a diode and can decrease substantially under reverse bias. As the amount of collected charge increases,  $V_{\text{pin}}$  is reduced as well, however this change is relatively small due to the high PPD capacitance created by the pinning p+ layer on top.

Figure 9 shows how the increasing reverse substrate bias pulls down  $V_{\text{pin}}$ . This simulates 18  $\mu\text{m}$  thick, 1  $\text{k}\Omega\cdot\text{cm}$  epitaxial layer which becomes fully depleted at  $V_{\text{BSB}} = -5\text{V}$ .

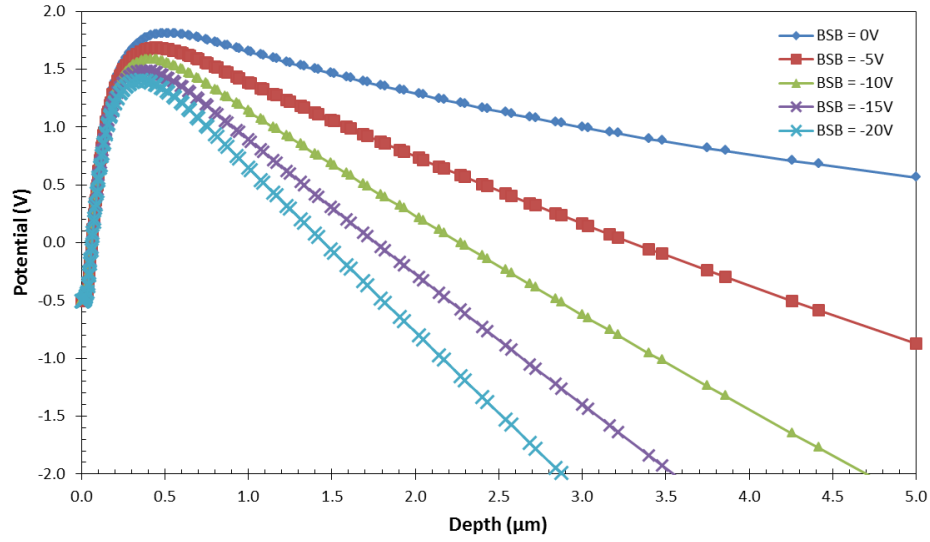


Figure 9 – Potential in depth under a PPD for increasing reverse substrate bias  $V_{BSB}$ .

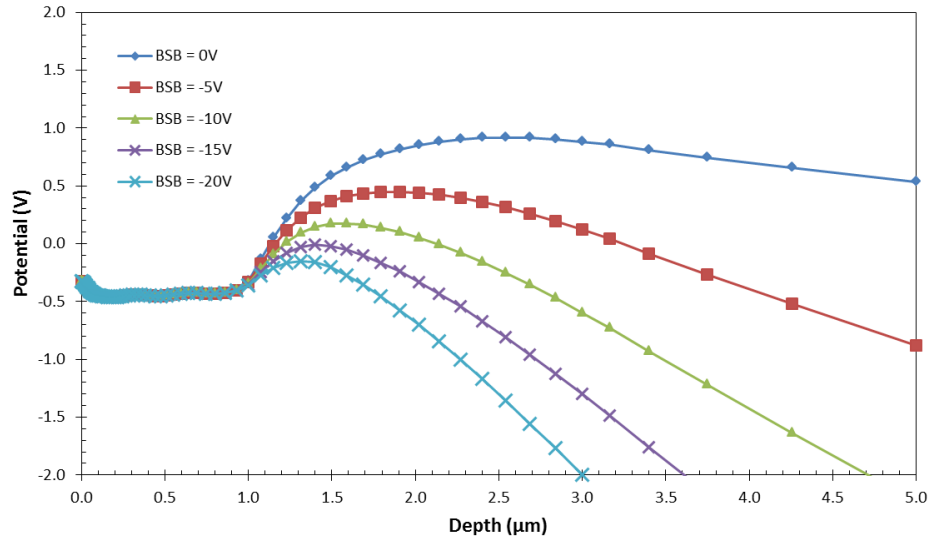


Figure 10 – Potential in depth under a p-well with a DDE underneath, for increasing substrate bias  $V_{BSB}$ .

Similarly, the reverse substrate bias affects the potential barrier under the in-pixel p-wells. At zero substrate bias the DDE helps create a potential barrier of the order of 1V under the p-wells. This barrier is sufficient to significantly suppress the parasitic leakage current due to the exponential dependence on the barrier height. As the simulation in Figure 10 shows, increasing reverse bias decreases the barrier height similarly to  $V_{pin}$  in Figure 9. At sufficiently high  $V_{BSB}$ , reverse current will begin to flow due to thermionic emission over the potential barrier. This condition, however, is distinct from breakdown and is a consequence of the way the potential barrier under the p-well is created. The ability to affect  $V_{pin}$  and the potential barrier under the p-well by the reverse bias could be used to fine tune the characteristics of the sensor if it has been designed to achieve over-depletion.



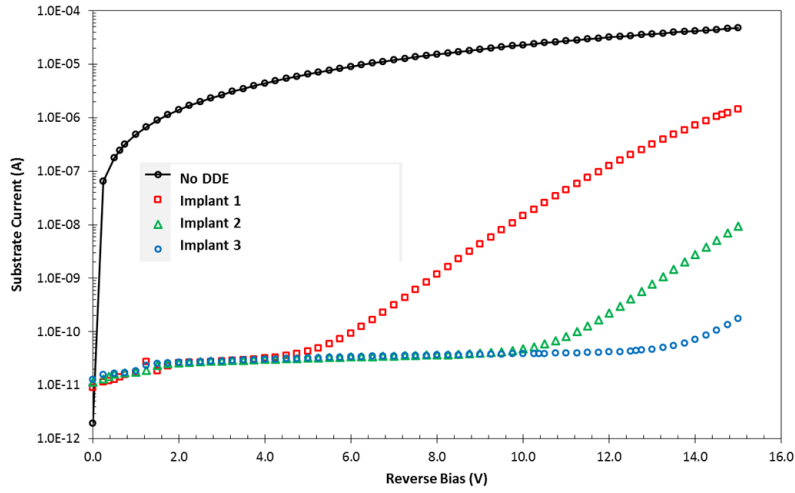


Figure 11 – Simulated substrate current for three different energies of the DDE implant and for no implant.

Some results from the optimisation of the DDE implant are shown in Figure 11. As the energy of the phosphorus implantation is increased for identically shaped implants, the potential barrier under the p-well increases, and this moves the onset of reverse current increase towards higher bias values. For comparison, the much higher reverse current when no DDE is present is also plotted. Finally, a range of DDE sizes, implantation doses and energies were chosen for manufacture, taking into account the constraints from using the existing CIS process and the challenges arising from the required high energy phosphorus implantation step.

The designed sensor is fully compatible with both NMOS and PMOS transistors outside the pixel area. Due to the reverse bias, all off-pixel MOSFETs in their local n- and p-wells reside on top of a deep n-well (Figure 12), which is available in the TowerJazz CIS process. In this way, all off-pixel circuitry appears as a reverse biased diode and collects photogenerated charge parasitically.

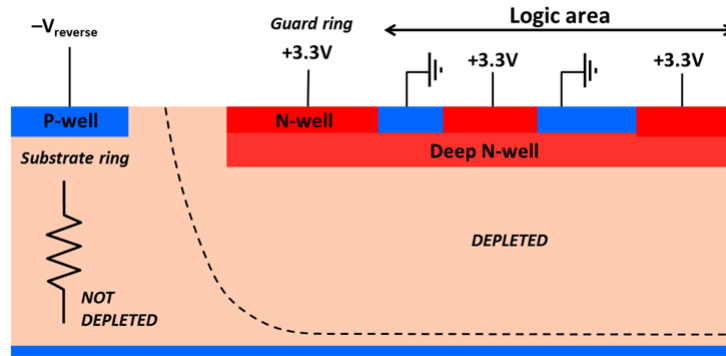


Figure 12 – Logic circuitry in the reverse biased CMOS sensor.

An unexpected complication from reverse biasing the substrate was that the standard electrostatic discharge (ESD) protection circuitry was no longer compatible. Double guard ring for electron and hole sinking is required for the ESD to be effective, and the circuits were redesigned to use p-wells connected to  $V_{BSB}$  for hole sinks. Electron sinks remained unchanged and used the existing n-wells as usual.

### 3.2 Manufacture

The first prototype device is presently being manufactured by TowerJazz Semiconductor. It is being made on epitaxial wafers with resistivity of 1 k $\Omega$ .cm and thickness of 18  $\mu$ m. This epi thickness was chosen because it is routinely used for

commercial devices and reduces the risk in manufacture. The proposed method of achieving full depletion by reverse biasing the substrate does not depend of the thickness of the active silicon, and can in principle be scaled up to hundreds of micrometers. With the chosen epi thickness the device operating principles can be studied and verified, and later implemented in much thicker, higher resistivity substrates.

The test chip consists of two pixel arrays with pitches of 10  $\mu\text{m}$  and 5.4  $\mu\text{m}$ , each with four different design variants for the DDE shape. In addition, a number of batch splits explores different energies for the DDE implant. The off-pixel circuitry is kept to the bare minimum, and only a row decoder and simple source follower buffers for the pixel signals are provided.

## CONCLUSIONS

A novel PPD pixel structure for achieving full depletion using reverse substrate bias is presented. The operating principle is based on extending the depletion regions from the PPDs under the in-pixel p-wells in order to achieve pinch-off and prevent parasitic substrate currents between the front and the back of the device. Only one additional implantation step is required in the manufacturing process to achieve this, and in principle very thick substrates of high resistivity silicon can be fully depleted.

Based on this approach, a prototype sensor has been designed by the CEI and is presently in manufacture by TowerJazz Semiconductor. A range of implantation process splits is being implemented to evaluate the technology in 10  $\mu\text{m}$  and 5.4  $\mu\text{m}$  pixel pitches.

We are expecting that this development will lead to the realization of PPD image sensors with much higher QE in the red and near-IR wavelengths, comparable to state of the art backside illuminated CCDs. This will complement the excellent electro-optical characteristics of PPD CIS, combined with their potential to achieve high frame rate, low power dissipation and functionality integration typical for CMOS imagers.

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